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Claims

[c1] An integrated circuit (IC) chip with circuits formed thereon, a plurality of chip interconnect pads formed on a surface of said IC chip, one or more of said plurality of chip interconnect pads being an electoplated pad, said electroplated pad having a plated layer plated to a platable pad.

[c2] An IC chip as in claim 1, wherein each said platable pad is disposed in a cavity in a chip surface and said plated layer is formed in said cavity.

[c3] An IC chip as in claim 2, wherein said plated layer is a noble metal plated layer and said noble metal is a metal selected from a group consisting of gold, platinum, palladium, rhodium, ruthenium, osmium, iridium and indium.

[c4] An IC chip as in claim 3, wherein said platable pad is a copper/nickel pad.

[c5] An IC chip as in claim 4, wherein noble metal is gold.

[c6] An IC chip as in claim 5, wherein each said electroplated pad includes a barrier metal layer, said barrier metal

layer being a non-platable conductive material layer at the perimeter of said electroplated pad and extending upward along a sidewall of said cavity and alongside said noble metal plated layer.

[c7] An IC chip as in claim 6, wherein said barrier metal is a metal selected from a group consisting of nickel (Ni), tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), aluminum (Al), tungsten (W), chromium (Cr) and titanium tungsten (TiW).

[c8] An IC chip as in claim 1, wherein said each plated pad further includes an electrical connection to an underlying strap, said underlying strap extending horizontally from said electrical connection to a chip side wall.

[c9] An IC chip as in claim 8, wherein said underlying strap extends beyond a crack stop ring.

[c10] An IC chip as in claim 8, wherein said underlying strap is a tungsten strap.

[c11] A semiconductor wafer with a plurality of die locations, each of said die locations being separated from other said die locations by a kerf space, said semiconductor wafer comprising:
a plurality of integrated circuit (IC) chips, each IC chip including a plurality of devices formed on a semiconduc-

tor surface of said semiconductor substrate in one of said die locations, said devices being wired together into a circuit, selected ones of said devices being connected to one of a plurality of chip pads;

a conductive grid line in each said kerf space;

a conductive ring, each said conductive grid line being connected to said conductive ring; and

a conductive strap connected to one of said plurality of chip pads on said each chip, each of said plurality of chip pads being connected to one said conductive strap, each said conductive strap being connected to an adjacent said conductive grid line, whereby a bias supply current provided to said conductive ring, passes through to each of said plurality of chip pads on said each chip.

[c12] A semiconductor wafer as in claim 11, further comprising:

a passivation layer covering said grid lines on an upper surface of said wafer, said conductive ring and at least a portion of said chip pads being exposed beneath said passivation layer.

[c13] A semiconductor wafer as in claim 12, further comprising:

a pad opening in said passivation layer at each of said chip pads, said pad opening exposing a corresponding one of said chip pads through said passivation layer.

[c14] A semiconductor wafer as in claim 13, further comprising:
a donut shaped barrier ring at each said pad opening, said corresponding one being exposed through the center of said donut shaped barrier ring.

[c15] A semiconductor wafer as in claim 13, further comprising:
a plurality of wiring layers between said devices and said chip pads, wiring in said plurality of wiring layers connecting each of said off-chip pads to a corresponding said conductive strap.

[c16] A semiconductor wafer as in claim 15, wherein conductive grid lines are in a layer between said passivation layer and a pad layer, said semiconductor wafer further comprising:
a conductive stud between each said conductive strap and said adjacent conductive grid line.

[c17] A semiconductor wafer as in claim 15, wherein said chip pads comprise a copper layer.

[c18] A semiconductor wafer as in claim 17, wherein said conductive ring and said conductive grid lines are of a conductive material selected from a group of materials consisting of nickel (Ni), Tantalum (Ta), Tantalum Nitride

(TaN), Titanium (Ti), Titanium Nitride (TiN), Aluminum (Al), Tungsten (W), Chromium (Cr) and Titanium Tungsten (TiW).

[c19] A semiconductor wafer as in claim 17, wherein said conductive straps are tungsten straps.

[c20] A semiconductor wafer as in claim 17, wherein said chip pads further comprise a noble metal layer.

[c21] A semiconductor wafer as in claim 20, wherein said noble metal is gold.

[c22] A semiconductor wafer as in claim 17, further comprising:
a crack stop ring around each of said plurality of IC chips, said crack stop ring disposed between adjacent said kerf space and an enclosed IC chip.

[c23] A method of forming integrated circuit (IC) chips on a semiconductor wafer, said method comprising the steps of:
a)forming devices in a semiconductor layer;
b)forming pad straps at said semiconductor layer;
c)forming wiring layers above said semiconductor layer, said wiring layers selectively wiring devices together;
d)forming barrier metal pads in a pad layer on said wiring layers;

e)forming a conductive terminal, wiring on said wiring layers connecting said conductive terminal to said barrier metal pads; and

f)plating said barrier metal pads with a noble metal.

[c24] A method of forming IC chips as in claim 23, wherein grid lines are formed between chips on said semiconductor wafer in the step (e) of forming the conductive terminal, said grid lines being connected to said conductive terminal.

[c25] A method of forming IC chips as in claim 24, wherein before the step (f) of plating said barrier metal pads, said method further comprises the step of:

f1)forming a crack stop ring around each of said IC chips.

[c26] A method of forming IC chips as in claim 24, wherein said conductive terminal is a conductive ring around said semiconductor wafer and before the step (f) of plating said barrier metal pads, said method further comprises the steps of:

f1)forming a passivation layer on said semiconductor wafer; and

f2)opening said passivation layer at said pads and said conductive terminal.

[c27] A method of forming IC chips as in claim 26, further comprising the step of:
f3)forming a donut shaped barrier ring at each open said pad.

[c28] A method of forming IC chips as in claim 23, further comprising the step of:
g)dicing said semiconductor wafer, said barrier metal connection to said conductive terminal and kerf connections to each strap being removed by dicing.